programmable devices; logic devices; gate arrays; ASICs (application specific integrated circuits); and microprocessors. The present invention is further suitable for use in any system or systems which employ such devices types.

While the invention has been particularly shown and described with reference to a preferred embodiment, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention. For instance, the address path circuitry shown in the figures is but one example of how the circuitry and methodology of the present invention may be implemented.

What is claimed is:

1. A method of internally controlling a clock signal of an integrated circuit device such that a data path of the integrated circuit device is initialized in a test mode, comprising the steps of:

upon a power-up condition in the test mode of the integrated circuit device forcing the clock signal of the integrated circuit device to a first logic state, thereby causing a master element of the integrated circuit device to load in first data and to conduct; and

upon completion of the power-up condition forcing the clock signal of the integrated circuit device to a second logic state, thereby latching In the first data to the master element and causing a slave element of the integrated circuit device to load in second data generated by the master element and to conduct.

2. The method of claim 1, wherein the first logic state is a low logic state and the second logic state is a high logic state.

3. The method of claim 1, wherein the power-up condition of the integrated circuit device is controlled by a power-on-reset signal of the integrated circuit device.

4. The method of claim 3, wherein the power-on-reset signal is an internally generated signal which changes logic state once a threshold value of a positive power supply is passed as the positive power supply rises.

5. The method of claim 1, wherein the clock signal of the integrated circuit device is an external clock signal of the integrated circuit device or a derivative signal of the external clock signal.

6. The method of claim 1, wherein the master element of the integrated circuit device is a master latch element and the slave element is a slave latch element.

7. The method of claim 1, wherein the master element of the integrated circuit device is a master flip-flop element and the slave element is a slave flip-flop element.

8. The method of claim 1, wherein upon the power-up condition of the integrated circuit device, the clock signal is internally clocked.

9. The method of claim 1, wherein when the master element is conducting the slave element does not conduct and when the slave element is conducting the master element does not conduct.

10. The method of claim 1, wherein the test mode is entered upon the power-up condition of the integrated circuit device.

11. The method of claim 1, wherein the data path is an address path.

12. The method of claim 1, wherein in the test mode the integrated circuit device is tested at a voltage above a normal operating voltage of the integrated circuit device.

13. The method of claim 12, wherein the clock signal is tested in both the first logic state and the second logic state at the voltage.

14. The method of claim 1, wherein the integrated circuit device is a synchronous clocked device.

15. The method of claim 1, wherein conduction of the master element and conduction of the slave element initializes an address path of the integrated circuit device such that a plurality of columns and a plurality of rows of the integrated circuit device are not selected.

16. The method of claim 1, wherein conduction of the master element and conduction of the slave element initial-

izes an address path of the integrated circuit device such that a plurality of columns and a plurality of rows of the integrated circuit device are selected.

17. The method of claim 16. wherein a plurality of bitlines true of the integrated circuit device are held at a first voltage level and a plurality of bitlines complement of the integrated circuit device are held at a second voltage level.

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